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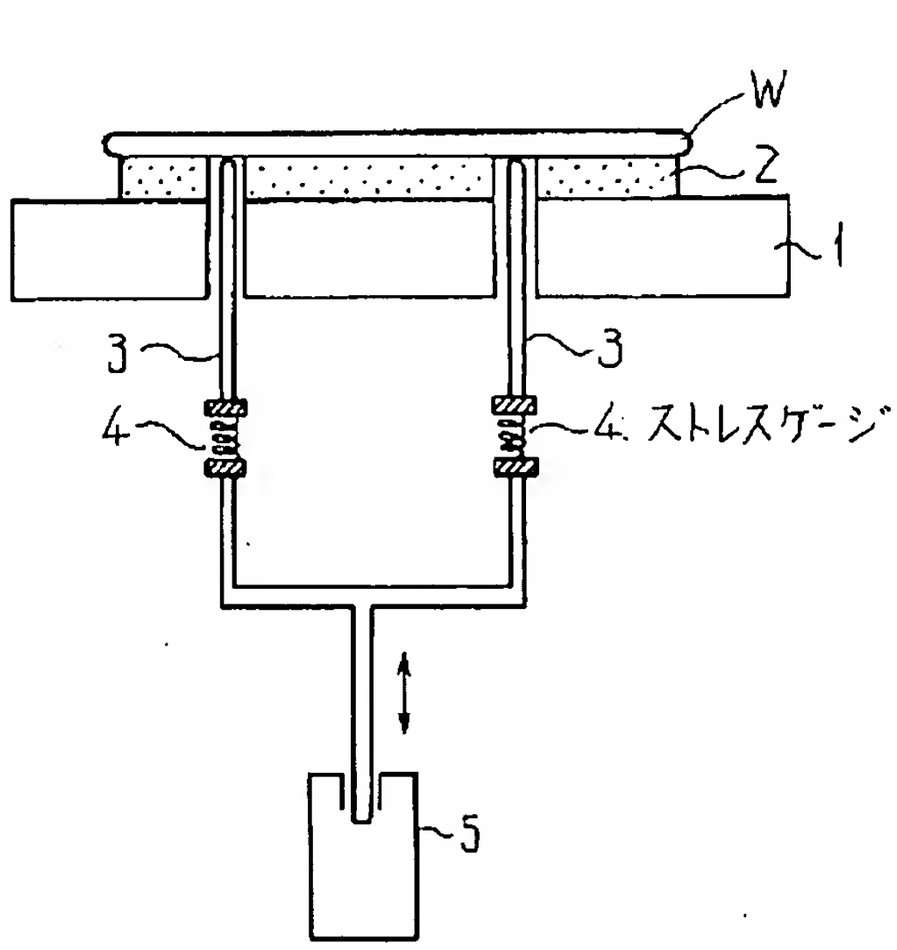
(54)【発明の名称】　静電チャック

(57)【要約】
【目的】　ウエハを支持する静電チャックに関し，静電チャックの固定電荷除去に要する時間のマージンを低減して，装置の稼働率および処理のスループットを向上させることを目的とする。
【構成】　１）ウエハを支持するウエハ支持台１と，該ウエハ支持台上で該ウエハを上下動させるリフトピン３と，該上下動の際に該リフトピンにかかるストレスを検知するストレスセンサ４とを有するように構成する。
２）前記ストレスセンサがスプリングを用いた接点式センサ，またはピエゾ素子，または圧力計であるように構成する。
３）前記ストレスセンサが出力する信号を，ウエハ搬送系を司るCPU に帰還し，ウエハ搬送の可，不可を判断する機能を有するように構成する。

本発明の原理説明図



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【特許請求の範囲】
【請求項１】　ウエハを支持するウエハ支持台と，該ウエハ支持台上で該ウエハを上下動させるリフトピンと，該上下動の際に該リフトピンにかかるストレスを検知するストレスセンサとを有することを特徴とする静電チャック。
【請求項２】　前記ストレスセンサがスプリングを用いた接点式センサ，またはピエゾ素子，または圧力計であることを特徴とする請求項１記載の静電チャック。
【請求項３】　前記ストレスセンサが出力する信号を，ウエハ搬送系を司るCPU に帰還し，ウエハ搬送の可，不可を判断する機能を有することを特徴とする静電チャック。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明はドライエッチング装置等においてウエハを支持する静電チャックに関する。
【０００２】近年，半導体装置の微細化に伴い，ドライエッチング装置ではウエハの冷却が重要視されている。そのためウエハを支持するウエハチャックは均一な温度分布を得ることおよびウエハとの間の熱抵抗が少なく熱伝導率が高いことである必要がある。
【０００３】従来，良く冷却されたウエハ支持台に単にウエハを置くだけでは，エッチング中にプラズマから供給される熱を充分に逃すことができず，エッチング特性の再現性が乏しかった。
【０００４】このために，ウエハ周辺をクランプし機械的に押しつけてウエハ支持台に熱を逃がす方法が実用化されているが，この方法はウエハのオリエンテーションフラットとクランプの位置合わせが必要となり，またウエハ周辺に約２㎜程度のクランプマージンが犠牲になり，さらにクランプの影響でウエハ周辺約５～７㎜程度の領域のエッチング特性が変化するため，デバイス形成領域を縮小していた。
【０００５】さらに最近では静電チャックを利用するようになった。静電チャックはウエハをクランプすることなくウエハからチャックへの熱伝達率を飛躍的に高くすることができるからである。
【０００６】
【従来の技術】図３(A),(B) は静電チャックの例を示す断面図である。図において，１はウエハ支持台，２は絶縁板，６はDC電極，７はDC電源，11は冷却器，Wはウエハである。
【０００７】図３(A) は１電極で片側接地型，図３(B) と２電極型である。ウエハWと電極６間にはセラミックスや絶縁性のゴムシート等からなる絶縁板２で電気的に絶縁されている。
【０００８】エッチング中にウエハWと電極６間にわずかの電流が流れ，図４に示されるように絶縁膜中に固定電荷が生ずる。図４(A),(B) は残留する固定電荷の説明

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図である。
【０００９】図４(A) はプラズマ処理装置の断面を含む構成図で，１は静電チャックのウエハ支持台でプラズマ発生用の基板側電極，２は絶縁板，６は静電チャックのDC電極，７は静電チャックのDC電源，８は高周波フィルタ，９はプラズマ発生用の対向電極，10はプラズマ発生用のRF電源，Wはウエハである。
【００１０】図中で，矢印は電子の通過経路を示す。図４(B) は絶縁膜中に残留する固定電荷の説明図である。ウエハ中にプラズマから電子が注入されると，ウエハおよび絶縁板中に電子－正孔対が発生し，電子はDC電極７より流出して正の電荷が残留する。
【００１１】固定電荷は，DC電圧を切った後も，またプラズマ発生用のRF電源を切った後もそのまま絶縁板２中に存在するため，ウエハは継続的に支持台に吸着されたままになる。この残留吸着力のために，ウエハ搬送時にウエハを離脱する際，ウエハは支持台上で跳ね上がり，位置ずれを生じ，搬送エラーを誘発する。
【００１２】この問題を防止するため，一般にはDC電圧を切った状態でプラズマ照射を行い，残留する固定電荷を除去する方法が採られている。残留する固定電荷量はエッチングするウエハの膜構造に依存するため，固定電荷除去プロセスは充分なマージンを持って行うことが必要である。
【００１３】
【発明が解決しようとする課題】従来の固定電荷除去プロセスでは充分なマージンを持って行うことが必要であり，その結果，処理のスループットを犠牲にしなければならないという問題があった。しかしながら，現状の技術では固定電荷の除去はこの方法にたよるしかなかった。
【００１４】本発明は静電チャックの固定電荷除去に要する時間のマージンを低減して，装置の稼働率と処理のスループットを向上させることを目的とする。
【００１５】
【課題を解決するための手段】上記課題の解決は，１）ウエハを支持するウエハ支持台と，該ウエハ支持台上で該ウエハを上下動させるリフトピンと，該上下動の際に該リフトピンにかかるストレスを検知するストレスセンサとを有する静電チャック，あるいは２）前記ストレスセンサがスプリングを用いた接点式センサ，またはピエゾ素子，または圧力計である前記１）記載の静電チャックにより達成される。３）前記ストレスセンサが出力する信号を，ウエハ搬送系を司るCPU に帰還し，ウエハ搬送の可，不可を判断する機能を有する静電チャックにより達成される。
【００１６】
【作用】図１(A),(B) は本発明の原理説明図である。図において，１は支持台，２は絶縁板でセラミックス板，３はリフトピン，４はストレスゲージ（ストレスセン

サ），5は昇降動力源，Wはウエハである。

【００１７】本発明ではウエハ離脱の際，まず，DC電源を切った状態でプラズマを印加して残留する固定電荷の除去プロセスを行う。ウエハが残留する固定電荷で強い吸着状態にあるときリフトピン3は上昇の途中でストレスゲージ4によりリフトピンにかかるストレスを検知し，この情報をリフトピンの動きを制御するCPU を経由して昇降動力源5の上昇を停止する。

【００１８】次いで，再度DC電源を切った状態でプラズマを印加して残留する固定電荷の除去プロセスを行う。次いで，リフトピン上昇途中でストレスを測定する。ストレスが一定限度以下でウエハを上昇できると後のシーケンスを進める。

【００１９】このようにして，ウエハ離脱の際の搬送エラーを撲滅し，残留電荷除去プロセス時間を低減して離脱シーケンスの見込むべきマージンを最小にして，装置の稼働率の向上，処理のスループットの向上が可能となる。

【００２０】

【実施例】図２（A)～(D）は本発明の実施例の説明図である。図２(A）はストレスゲージとしてスプリングを用い，リフトピンの上下方向の変移αが一定値に達したときに，電流が流れる接点を利用した例である。

【００２１】図２(B）はリフトピンの上下方向の変移αに対するストレスF(α）の関係を示す図で，$\alpha=\alpha_0$ に対するF(α_0)より大きいストレスでは搬送エラーが誘発され，F(α_0)より小さいストレスでは正常な状態である。

【００２２】図２(C）はストレスをピエゾ素子を用いて検出する例，図３(D）はストレスを圧力計を用いて検出する例である。以上いずれのストレスゲージを用いても，前記のようにその出力を電気信号に変換し，ウエハの搬送系を制御するCPU に帰還し，ウエハ搬送の全体のタイミングを適当に調整する。

【００２３】また，ストレスゲージの出力を期待される標準出力と比較し，異常があれば警報を発するようにしてもよい。

【００２４】

【発明の効果】本発明によれば，静電チャックの固定電荷除去に要する時間のマージンを低減して，装置の稼働率と処理のスループットを向上させることができた。

【図面の簡単な説明】

【図１】　本発明の原理説明図

【図２】　本発明の実施例の説明図

【図３】　静電チャックの例を示す断面図

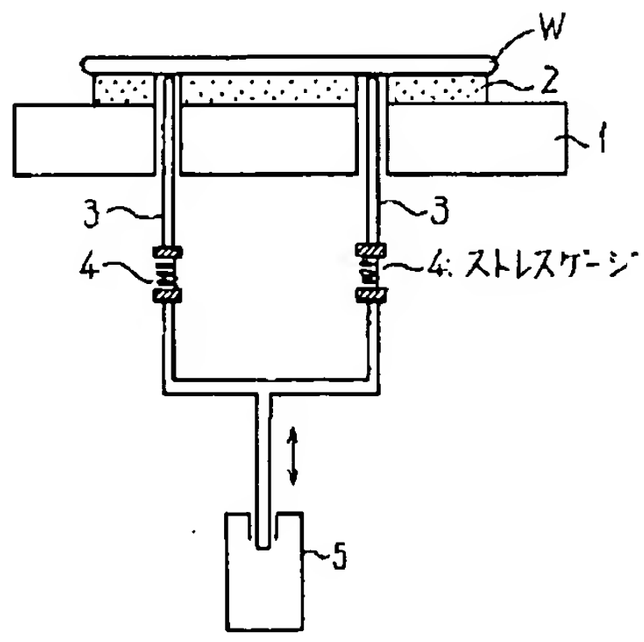
【図４】　残留する固定電荷の説明図

【符号の説明】

1　支持台
2　絶縁板でセラミックス板
3　リフトピン
4　ストレスゲージ
5　昇降動力源
6　静電チャックのDC電極
7　静電チャックのDC電源
8　高周波フィルタ
9　プラズマ発生用の対向電極
10　プラズマ発生用のRF電源
11　冷却器
W　ウエハ

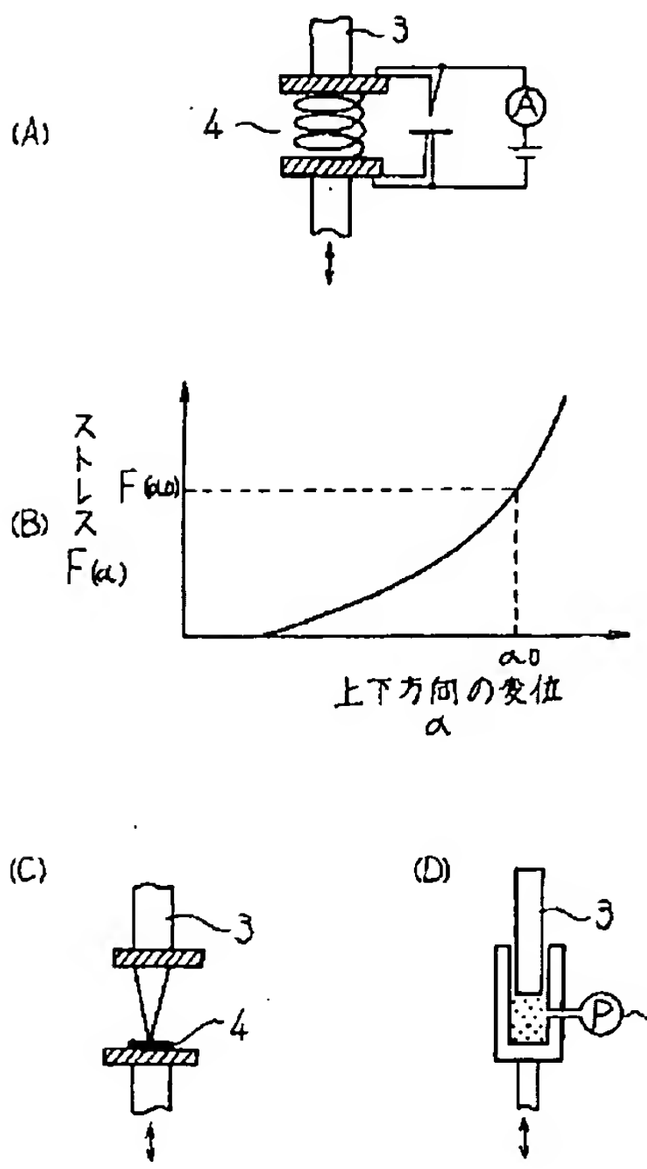
【図１】

本発明の原理説明図



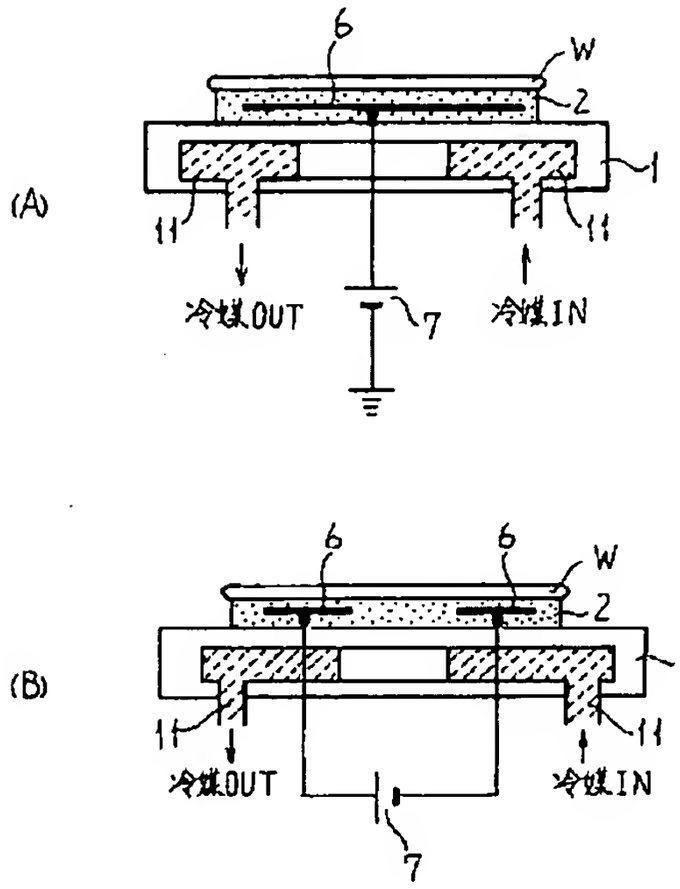
【図2】

実施例の説明図



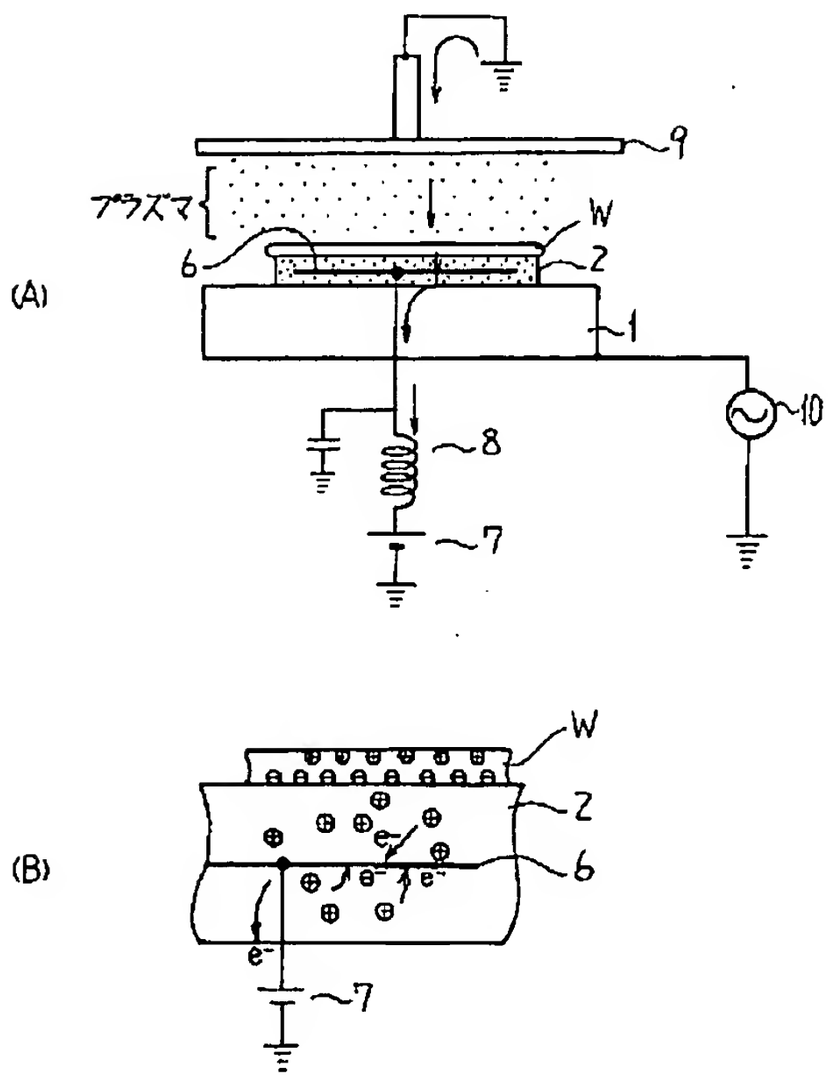
【図3】

静電チャックの例を示す断面図



【図4】

残留する固定電荷・説明図



PATENT ABSTRACTS OF JAPAN

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(71)Applicant : FUJITSU LTD

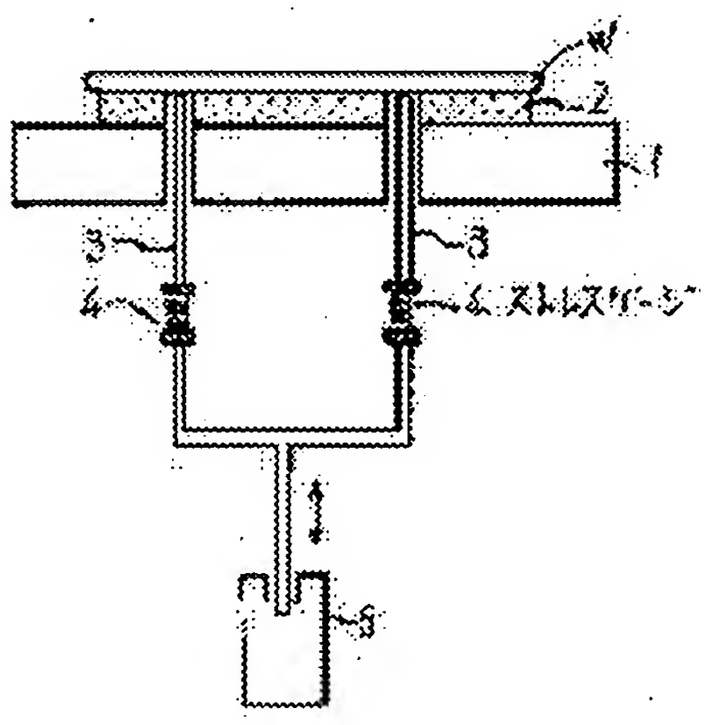
(72)Inventor : MATSUNAGA DAISUKE

(54) ELECTROSTATIC CHUCK

(57)Abstract:

PURPOSE: To reduce the margin for the time necessary to elimination of fixed charge of an electrostatic chuck, and improve the operating efficiency of an equipment and the throughput of processing.

CONSTITUTION: The following are provided for constitution; a wafer retaining stand 1 retaining a wafer, lift pins 3 moving the wafer vertically on the wafer retaining stand, and stress sensors 4 detecting the stress applied to the lift pins at the time of vertical movement. The stress sensor is a contact type sensor using a spring, or a piezoelectric element, or a pressure gauge. The signal outputted from the stress sensor is fed back to a CPU governing wafer conveyance, which CPU is constituted so as to have a function to judge whether wafer conveyance is allowable.



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[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] Wafer susceptor which supports a wafer, Electrostatic chuck characterized by having the lift pin which moves this wafer up and down on this wafer susceptor, and the stress sensor which detects the stress which starts this lift pin in the case of this vertical movement.
[Claim 2] Contact type sensor [sensor / said / stress] using a spring, Or piezo-electric element, Or electrostatic chuck according to claim 1 characterized by being a manometer.
[Claim 3] CPU which manages a wafer conveyance system for the signal which said stress sensor outputs It returns and is good [of wafer conveyance], Electrostatic chuck characterized by having the function to judge a failure.

[Translation done.]

* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the electrostatic chuck which supports a wafer in a dry etching system etc.
[0002] In recent years, with the dry etching system, importance is attached to cooling of a wafer with detailed-izing of a semiconductor device. Therefore, the wafer chucks which support a wafer need to be acquiring uniform temperature distribution and that there is little thermal resistance between wafers and thermal conductivity is high.
[0003] Only by putting a wafer on the wafer susceptor cooled well conventionally, the heat supplied from the plasma during etching could not fully be missed, but the repeatability of an etching property was scarce.
[0004] For this reason, although the approach of clamping the wafer circumference, pushing mechanically and missing heat to wafer susceptor was put in practical use, since the orientation flat of a wafer and the alignment of a clamp were needed, and about 2mm clamp margin fell victim around a wafer and the etching property of the field of about about 5-7mm of wafer circumferences changed under the effect of a clamp further, this approach was reducing the device formation field.
[0005] Furthermore, recently, it came to use an electrostatic chuck. It is because an electrostatic chuck can make high the heat transfer rate from a wafer to a chuck by leaps and bounds, without clamping a wafer.
[0006]
[Description of the Prior Art] Drawing 3 (A) and (B) It is the sectional view showing the example of an electrostatic chuck. drawing -- setting -- 1 -- wafer susceptor and 2 -- an electric insulating plate -- for 6, DC electrode and 7 are [a condensator and W of a DC power supply and 11] wafers.
[0007] Drawing 3 (A) They are a single-sided touch-down mold and drawing 3 (B) with one electrode. They are 2 electrode molds. Between Wafer W and the electrode 6, it insulates electrically with the electric insulating plate 2 which consists of ceramics, an insulating rubber sheet, etc.
[0008] Few currents between Wafer W and an electrode 6 flow during etching, and as shown in drawing 4 , a fixed charge arises in an insulator layer. Drawing 4 (A) and (B) It is the explanatory view of the fixed charge which remains.
[0009] Drawing 4 (A) It is a block diagram including the cross section of plasma treatment equipment, and, for 1, the substrate lateral electrode for plasma generating and 2 are [DC electrode of an electrostatic chuck, RF power source for / 7 / plasma generating in the DC power supply of an electrostatic chuck, the counterelectrode for / 8 / plasma generating in a high pass filter and 9, and 10, and W of an electric insulating plate and 6] wafers in the wafer susceptor of an electrostatic chuck.
[0010] All over drawing, an arrow head shows an electronic transit route. Drawing 4 R> 4 (B) It is the explanatory view of the fixed charge which remains in an insulator layer. If an electron is poured in from the plasma into a wafer An electronic-electron hole pair occurs in a wafer and an electric insulating plate, an electron flows out from the DC electrode 7, and positive charge remains.,

[0011] Even after the fixed charge cut DC electrical potential difference Since it exists in an electric insulating plate 2 as it is even after shutting off RF power source for plasma generating again, a wafer is left with the susceptor adsorbed continuously., To a this residual adsorption force sake When seceding from a wafer at the time of wafer conveyance A wafer leaps up on susceptor, A location gap is produced, A conveyance error is induced.,
[0012] In order to prevent this problem, a plasma exposure is performed where DC electrical potential difference is generally cut, The method of removing the fixed charge which remains is taken. As for the amount of fixed charges which remains, in order to be dependent on the membrane structure of the wafer to etch, a fixed charge removal process needs to carry out with sufficient margin.
[0013]
[Problem(s) to be Solved by the Invention] It is required to carry out with margin sufficient in the conventional fixed charge removal process, and it is the result, There was a problem that the throughput of processing had to be sacrificed. While carrying out a deer With the present technique, it could not but depend for removal of a fixed charge on this approach.,
[0014] This invention reduces the margin of the time amount which fixed charge removal of an electrostatic chuck takes, It aims at raising the operating ratio of equipment, and the throughput of processing.
[0015]
[Means for Solving the Problem] wafer susceptor to which solution of the above-mentioned technical problem supports one wafer, the electrostatic chuck which has the lift pin which moves this wafer up and down on this wafer susceptor, and the stress sensor which detects the stress which starts this lift pin in the case of this vertical movement, or 2 -- contact type sensor [sensor / said / stress] using a spring, Or piezo-electric element, Or it is attained by the electrostatic chuck of said one publication which is a manometer. 3) CPU which manages a wafer conveyance system for the signal which said stress sensor outputs It returns and is good [of wafer conveyance], It is attained by the electrostatic chuck which has the function to judge a failure.
[0016]
[Function] Drawing 1 (A) and (B) It is the principle explanatory view of this invention. drawing -- setting -- 1 -- for a ceramic plate and 3, a lift pin and 4 are [susceptor and 2 / a vertical movement power unit and W of a stress gage (stress sensor) and 5] wafers in an electric insulating plate.
[0017] the time of wafer balking in this invention -- first The removal process of the fixed charge which impresses the plasma and remains where a DC power supply is shut off is performed. It is CPU which the lift pin 3 detects the stress which starts a lift pin with the stress gage 4 in the middle of a rise, and controls a motion of a lift pin for this information when it is in a strong adsorbed state with the fixed charge with which a wafer remains. It goes and the rise of the vertical movement power unit 5 is suspended.
[0018] Subsequently, the removal process of the fixed charge which impresses the plasma and remains where a DC power supply is shut off again is performed. It ranks second, It is in the middle of a lift pin rise, and stress is measured. A next sequence will be advanced if stress can go up a wafer below in a fixed limit.
[0019] Thus, the conveyance error in the case of wafer balking is eradicated, and the margin which should reduce residual-charge removal process time amount, and should expect a balking sequence is made into min, Improvement in the operating ratio of equipment, Improvement in the throughput of processing is attained.
[0020]
[Example] Drawing 2 (A) - (D) It is the explanatory view of the example of this invention. Drawing 2 (A) When the change alpha of the vertical direction of a lift pin reaches constant value, using a spring as a stress gage, it is an example using the contact at which a current flows.
[0021] Drawing 2 (B) Stress F to the change alpha of the vertical direction of a lift pin (alpha) It is drawing showing relation, Alpha=alpha 0 For larger stress than receiving F (alpha 0), a conveyance error is induced and it is in a condition normal for stress smaller than F (alpha 0).

[0022] Drawing 2 (C) The example and drawing 3 (D) which detect stress using a piezo-electric element It is the example which detects stress using a pressure gage. CPU which changes the output into an electrical signal as mentioned above, and controls the conveyance system of a wafer even if it uses which stress gage above It returns and the timing of the whole wafer conveyance is adjusted suitably.
[0023] moreover As long as it is abnormal, you may make it emit an alarm as compared with the standard output from which the output of a stress gage is expected.
[0024]
[Effect of the Invention] According to this invention, the margin of the time amount which fixed charge removal of an electrostatic chuck takes is reduced, The operating ratio of equipment and the throughput of processing were able to be raised.

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TECHNICAL FIELD

[Industrial Application] This invention relates to the electrostatic chuck which supports a wafer in a dry etching system etc.

[0002] In recent years, with the dry etching system, importance is attached to cooling of a wafer with detailed-izing of a semiconductor device. Therefore, the wafer chucks which support a wafer need to be acquiring uniform temperature distribution and that there is little thermal resistance between wafers and thermal conductivity is high.

[0003] Only by putting a wafer on the wafer susceptor cooled well conventionally, the heat supplied from the plasma during etching could not fully be missed, but the repeatability of an etching property was scarce.

[0004] For this reason, although the approach of clamping the wafer circumference, pushing mechanically and missing heat to wafer susceptor was put in practical use, since the orientation flat of a wafer and the alignment of a clamp were needed, and about 2mm clamp margin fell victim around a wafer and the etching property of the field of about about 5-7mm of wafer circumferences changed under the effect of a clamp further, this approach was reducing the device formation field.

[0005] Furthermore, recently, it came to use an electrostatic chuck. It is because an electrostatic chuck can make high the heat transfer rate from a wafer to a chuck by leaps and bounds, without clamping a wafer.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] Drawing 3 (A) and (B) It is the sectional view showing the example of an electrostatic chuck. drawing -- setting -- 1 -- wafer susceptor and 2 -- an electric insulating plate -- for 6, DC electrode and 7 are [a condensator and W of a DC power supply and 11] wafers.
[0007] Drawing 3 (A) They are a single-sided touch-down mold and drawing 3 (B) with one electrode. They are 2 electrode molds. Between Wafer W and the electrode 6, it insulates electrically with the electric insulating plate 2 which consists of ceramics, an insulating rubber sheet, etc.
[0008] Few currents between Wafer W and an electrode 6 flow during etching, and as shown in drawing 4 , a fixed charge arises in an insulator layer. Drawing 4 (A) and (B) It is the explanatory view of the fixed charge which remains.
[0009] Drawing 4 (A) It is a block diagram including the cross section of plasma treatment equipment, and, for 1, the substrate lateral electrode for plasma generating and 2 are [DC electrode of an electrostatic chuck, RF power source for / 7 / plasma generating in the DC power supply of an electrostatic chuck, the counterelectrode for / 8 / plasma generating in a high pass filter and 9, and 10, and W of an electric insulating plate and 6] wafers in the wafer susceptor of an electrostatic chuck.
[0010] All over drawing, an arrow head shows an electronic transit route. Drawing 4 R> 4 (B) It is the explanatory view of the fixed charge which remains in an insulator layer. If an electron is poured in from the plasma into a wafer An electronic-electron hole pair occurs in a wafer and an electric insulating plate, an electron flows out from the DC electrode 7, and positive charge remains.,
[0011] Even after the fixed charge cut DC electrical potential difference Since it exists in an electric insulating plate 2 as it is even after shutting off RF power source for plasma generating again, a wafer is left with the susceptor adsorbed continuously., To a this residual adsorption force sake When seceding from a wafer at the time of wafer conveyance A wafer leaps up on susceptor, A location gap is produced, A conveyance error is induced.,
[0012] In order to prevent this problem, a plasma exposure is performed where DC electrical potential difference is generally cut, The method of removing the fixed charge which remains is taken. As for the amount of fixed charges which remains, in order to be dependent on the membrane structure of the wafer to etch, a fixed charge removal process needs to carry out with sufficient margin.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, the margin of the time amount which fixed charge removal of an electrostatic chuck takes is reduced, The operating ratio of equipment and the throughput of processing were able to be raised.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] It is required to carry out with margin sufficient in the conventional fixed charge removal process, and it is the result, There was a problem that the throughput of processing had to be sacrificed. While carrying out a deer With the present technique, it could not but depend for removal of a fixed charge on this approach.,
[0014] This invention reduces the margin of the time amount which fixed charge removal of an electrostatic chuck takes, It aims at raising the operating ratio of equipment, and the throughput of processing.

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MEANS

[Means for Solving the Problem] wafer susceptor to which solution of the above-mentioned technical problem supports one wafer, the electrostatic chuck which has the lift pin which moves this wafer up and down on this wafer susceptor, and the stress sensor which detects the stress which starts this lift pin in the case of this vertical movement, or 2 -- contact type sensor [sensor / said / stress] using a spring, Or piezo-electric element, Or it is attained by the electrostatic chuck of said one publication which is a manometer. 3) CPU which manages a wafer conveyance system for the signal which said stress sensor outputs It returns and is good [of wafer conveyance], It is attained by the electrostatic chuck which has the function to judge a failure.

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OPERATION

[Function] Drawing 1 (A) and (B) It is the principle explanatory view of this invention. drawing -- setting -- 1 -- for a ceramic plate and 3, a lift pin and 4 are [susceptor and 2 / a vertical movement power unit and W of a stress gage (stress sensor) and 5] wafers in an electric insulating plate.

[0017] the time of wafer balking in this invention -- first The removal process of the fixed charge which impresses the plasma and remains where a DC power supply is shut off is performed. It is CPU which the lift pin 3 detects the stress which starts a lift pin with the stress gage 4 in the middle of a rise, and controls a motion of a lift pin for this information when it is in a strong adsorbed state with the fixed charge with which a wafer remains. It goes and the rise of the vertical movement power unit 5 is suspended.

[0018] Subsequently, the removal process of the fixed charge which impresses the plasma and remains where a DC power supply is shut off again is performed. It ranks second, It is in the middle of a lift pin rise, and stress is measured. A next sequence will be advanced if stress can go up a wafer below in a fixed limit.

[0019] Thus, the conveyance error in the case of wafer balking is eradicated, and the margin which should reduce residual-charge removal process time amount, and should expect a balking sequence is made into min, Improvement in the operating ratio of equipment, Improvement in the throughput of processing is attained.

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EXAMPLE

[Example] Drawing 2 (A) - (D) It is the explanatory view of the example of this invention. Drawing 2 (A) When the change alpha of the vertical direction of a lift pin reaches constant value, using a spring as a stress gage, it is an example using the contact at which a current flows.
[0021] Drawing 2 (B) Stress F to the change alpha of the vertical direction of a lift pin (alpha) It is drawing showing relation, Alpha=alpha 0 For larger stress than receiving F (alpha 0), a conveyance error is induced and it is in a condition normal for stress smaller than F (alpha 0).
[0022] Drawing 2 (C) The example and drawing 3 (D) which detect stress using a piezo-electric element It is the example which detects stress using a pressure gage. CPU which changes the output into an electrical signal as mentioned above, and controls the conveyance system of a wafer even if it uses which stress gage above It returns and the timing of the whole wafer conveyance is adjusted suitably.
[0023] moreover As long as it is abnormal, you may make it emit an alarm as compared with the standard output from which the output of a stress gage is expected.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The principle explanatory view of this invention
[Drawing 2] The explanatory view of the example of this invention
[Drawing 3] The sectional view showing the example of an electrostatic chuck
[Drawing 4] The explanatory view of the fixed charge which remains
[Description of Notations]
1 Susceptor
2 It is Electric Insulating Plate and is Ceramic Plate.
3 Lift Pin
4 Stress Gage
5 Vertical Movement Power Unit
6 DC Electrode of Electrostatic Chuck
7 DC Power Supply of Electrostatic Chuck
8 High Pass Filter
9 Counterelectrode for Plasma Generating
10 RF Power Source for Plasma Generating
11 Condensator
W Wafer

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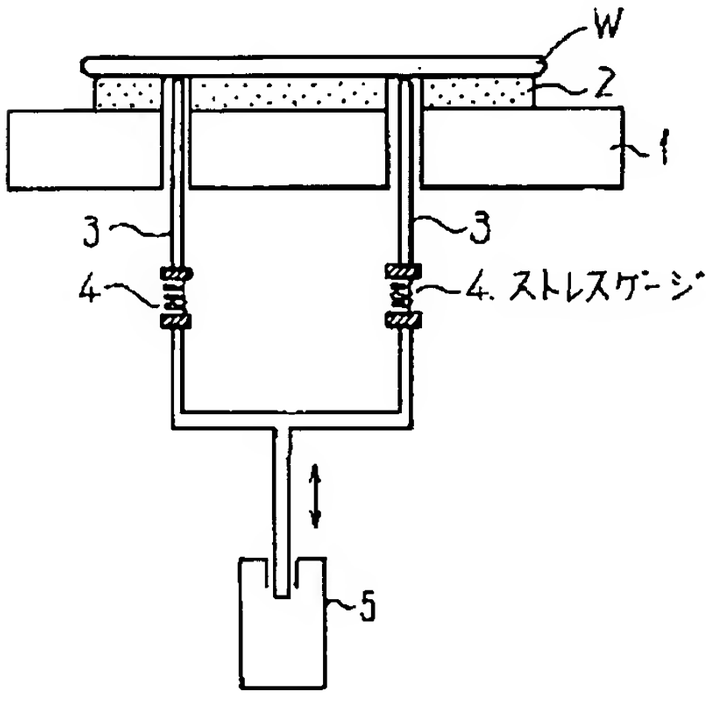
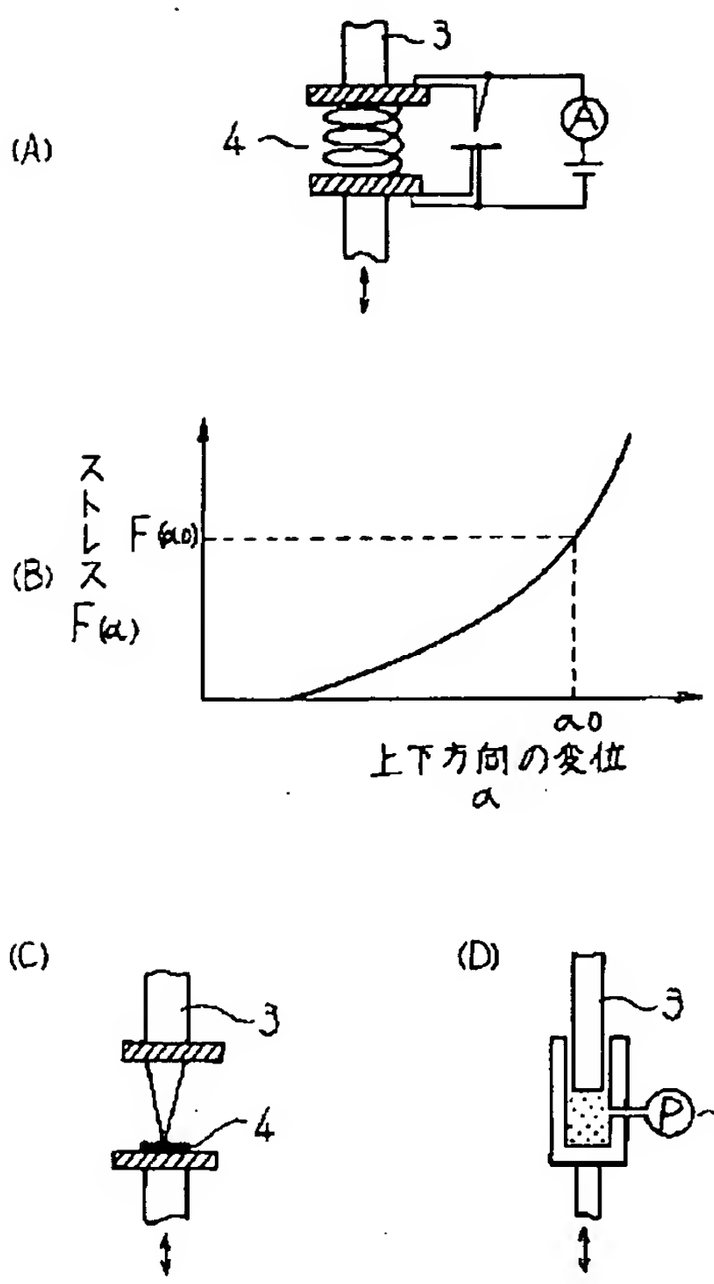
DRAWINGS

[Drawing 1]
本発明の原理説明図



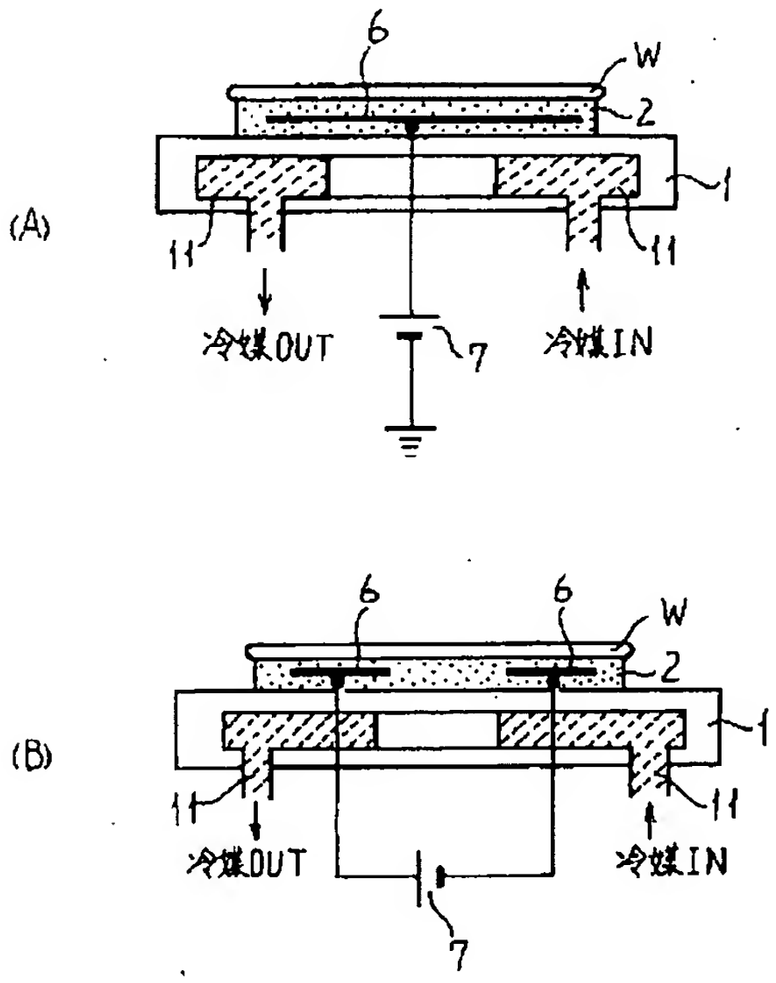
[Drawing 2]

実施例の説明図



[Drawing 3]

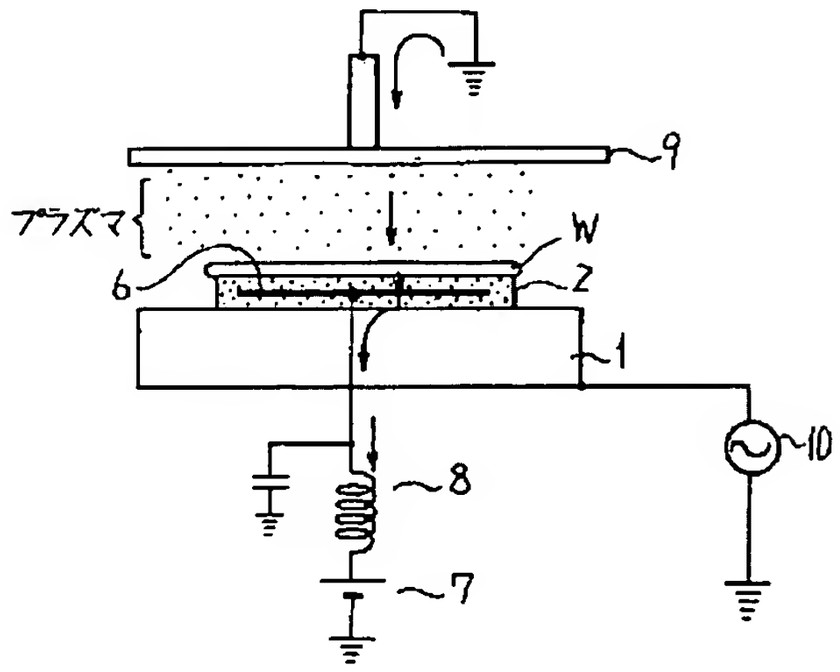
静電チャックの例を示す断面図



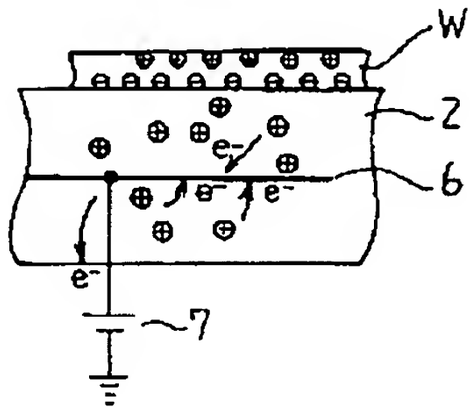
[Drawing 4]

残留する固定電荷・説明図

(A)



(B)



[Translation done.]